Rev. 8-83) U.S. Department of Communics Patent and Trademark Office (Rev. 8-83) Atty Docket 0819-0724 Serial No. 10/019,540 Applicants: Takashi NISHIKAWA Filiap Date: January 03, 2002 Group Art Unit: NIA Applicants: Takashi NISHIKAWA Filiap Date: January 03, 2002 Group Art Unit: NIA FOREIGN PATENT DOCUMENTS Country Class Subclass Translation Part Eng OTHER DOCUMENT (Including Author, Title, Date, Pertinent Pages, Etc.) Examiner Initial Table 22 Thermal/Thin Films Gate Etch and Doping Technology Requirement", p. 74, The National Technology Roadmap for Semiconductors Technology Needs Mornose et al., "Prospects for Low-Power, High-Speed MPU's Using 1.5 nm Direct Tunneling Gate Oxide Morses et al., "Prospects for Low-Power, High-Speed MPU's Using 1.5 nm Direct Tunneling Gate Oxide Morses et al., "Stacked High-4 Gate Dielectric for Gigascale Integration of Metal-Oxide-Semiconductor Technologies", pp. 2835-2837, June 1, 1998, Applied Physics Letters Vol. 72, No. 22 I. Sasaki et al., "Preparation and Characterization of ZT This Pilms on CeO ₆ (111)/Si(111) Structures", pp. 4987-4990, September 1996, Jpn. J. Appl. Phys. Vol. 35 T. Lei et al., "Epitable Growth and Characterization of ZT This Pilms on CeO ₆ (111)/Si(111) Structures", pp. 4933-4943, May 15, 1992, J. Appl. Phys. Vol. 71, No. 10 H. Minoda, "Nihon Butsuri Gakkaishi", pp. 244-250, 1999, Vol. 53 (with translation) K. Sakamoto et al., "Kotai Butsuri", pp. 559-564, 1994, Vol. 29, No. 6 (with translation)							Sheet 1 of	
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				Filing Date	January 3, 2002	
STATEMENT BY APPLICANT				First Named Inventor	Takashi NISHIKAWA	
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